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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,764	11/25/2003	Masashi Yonemaru	829-618	3114

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,764	YONEMARU, MASASHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,7 and 9-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/17/06 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

It is possible that one might interpret the "connected directly in series" language in amended claim 1 to include the "negative" requirement that no circuit elements be allowed between the claimed first and second PMOS or NMOS transistors. To the extent that such interpretation is intended (see Applicant's 10/17/06 remarks), claims 1,6, and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant's invention, as filed, contains no hint of a ("negative") requirement that no circuit elements be allowed between the claimed first and second PMOS or NMOS transistors. In his remarks, Applicant suggests that his initially filed figures 2B, 5B, 10B, and 13B-15B, with no textual explanation whatsoever,

suffice to show Applicant in possession of an invention with said negative limitation. Applicant is mistaken. Initially filed figures 2B, 5B, 10B, and 13B-15B, taken by themselves, show Applicant in possession of an invention with the series connected NMOS or PMOS transistors and additional circuit elements that optionally may, or optionally may not, be formed between (with the figures showing an embodiment where the second option has been chosen). Generally speaking, the mere absence of an initial positive recitation is not a basis for later claiming exclusion. See MPEP § 2173.05(i).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1,6, and 8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Yoon et al. (2004/0071013).

Yoon et al. discloses a semiconductor integrated circuit comprising a first cell 500-502-522 comprising a plurality of transistors including a PMOS transistor 526 and an NMOS transistor 530; a second cell 580 comprising a PMOS transistor section M15-

M19P, the PMOS transistor section M15-M19P comprising a first PMOS transistor M19P and a second PMOS transistor M15 connected to the first PMOS transistor M19P directly in series, and an NMOS transistor section M16-M19N, the NMOS transistor section M16-M19N comprising a first NMOS transistor M19N and a second NMOS transistor M16 connected to the first NMOS transistor M19N directly in series, wherein a predetermined scheme is used to connect between the first cell 500-502-522 and the second cell 580, between the plurality of transistors in the first cell 500-502-522, and between the PMOS transistor section M15-M19P and the NMOS transistor section M16-M19N in the second cell 580, wherein the first cell 500-502-522 functions as a logic operation circuit 501 for outputting data; and the second cell 580 functions as a driver circuit (note paragraph 0039) for driving the logic operation circuit 501 and as a data retaining circuit (again, note paragraph 0039) for retaining data output (via sense sub-circuit 500) by the logic operation circuit 501; the first PMOS transistor M19P, the second PMOS transistor M15, the first NMOS transistor M19N, and the second NMOS transistor M16 each comprise a gate 34, a source 32, and a drain 32; a first source 32 voltage may be applied via bit line 26 to the source 32 of the first PMOS transistor M19P; a second source 32 voltage may be applied via bit line 26 to the source 32 of the first NMOS transistor M19N; one of the gate 34 of the first PMOS transistor M19P and the gate 34 of the second PMOS transistor M15 may be connected via word lines 28 or 30 to an input terminal, an input signal PRT being input to the input terminal of second

PMOS transistor M15, and the other (first PMOS transistor M19P) is connected to a first gate control signal input terminal, a first gate control signal PWTb being input to the first gate control signal input terminal; one of the gate 34 of the first NMOS transistor M19N and the gate 34 of the second NMOS transistor M16 is connected to the input terminal PRT, and the other (first NMOS transistor M19N) is connected to a second gate control signal input terminal, a second gate control signal PWT being input to the second gate control signal input terminal; and the drain 32 of the second PMOS transistor M15 and the drain 32 of the second NMOS transistor M16 are connected to an output terminal 644. Note figures 5 and 6 and paragraphs 0039-0043 and 0071-0081 of Yoon et al.

Response to Arguments

5. Applicant's arguments filed 10/17/06 have been fully considered but they are not persuasive.

It is argued, at pages 10-11 of the remarks, that "claim 1 has been amended to require that (1) the first and second NMOS transistors are directly connected to each other in series and/or (2) the first and second PMOS transistors are directly connected to each other in series [with the intention] to prevent the Examiner from contending that in Fig. 6 of Yoon elements M16 and M19N are the claimed first and second NMOS transistors, and/or from contending that M15 and M19P are the claimed first and second PMOS transistors [because i]n Fig. 6 of Yoon, the PMOS transistor M15 of M16 and the

PMOS transistor M 19P are not connected directly in series... because inverter devices M17, M18 and driver-register circuit 618 are provided therebetween." This argument unfortunately is directly coupled to interpreting the new "directly connected" language as creating a limitation that prohibits the claimed device from having particular configurations. As explained above, no such prohibitions are found in the application as filed.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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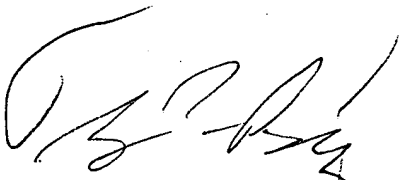
If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisors, Wael M Fahmy (571-272-1705) or Robert J. Pascal (571-272-1769). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Primary Examiner
Art Unit 2826